

**CLAIMS**

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[Claim(s)]

[Claim 1] It is the protected solar cell circuit. : The first photo voltaic cell;  
The first (coupled) contact combined with said first photo voltaic cell;  
The second photo voltaic cell that overlays said at least a part of first photo voltaic cell;  
A cap layer which overlays said at least a part of second photo voltaic cell;  
An epitaxial growth diode which said cap layer overlays in part at least;  
The second contact formed on [ at least some ] said cap layer;  
The first conductor that combines said diode electrically to said first contact; it reaches. A solar cell circuit where said diode operates as a by-pass diode to the first and the second photo voltaic cell including the second conductor that combines said by-pass diode with said second contact electrically.

[Claim 2] a solar cell circuit -- at least -- the -- the protected solar cell circuit according to claim 1 which is formed from III fellows and the Vth group element.

[Claim 3] The protected solar cell circuit according to claim 1 which has a window layer arranged between said cap layer and the second photo voltaic cell.

[Claim 4] The protected solar cell circuit according to claim 1 which contains a germanium substrate further.

[Claim 5] The protected solar cell circuit according to claim 1 which contains a GaAs substrate further.

[Claim 6] The protected solar cell circuit according to claim 1 which contains an insulating base material further.

[Claim 7] A by-pass diode optimizes for the universes to an operation under the AMO environment. (space qualified) The protected solar cell circuit according to claim 1 which was carried out.

[Claim 8] It is a solar cell circuit. : A multi-junction solar cell device which has at least two photo voltaic cells; it reaches. In order to protect the first and the second photo voltaic cell at least between at least two aforementioned photo voltaic cells. A solar cell circuit containing the first by-pass diode that grew said multi-junction solar cell portion epitaxially.

[Claim 9] The solar cell circuit according to claim 8 where said multi-junction solar cell portion contains the first cell and the second cell at least, and the first by-pass diode portion includes the first contact and the second contact.

[Claim 10] The third contact combined with said first cell;

A cap layer which overlays said at least a part of second cell;

The fourth contact combined with said cap layer;

The first conductor that combines the first contact and said third contact; it reaches. The solar cell circuit according to claim 9 which contains further the second conductor that combines said fourth contact and the second contact.

[Claim 11] The solar cell circuit according to claim 10 where the fourth contact is arranged at a pars basilaris ossis occipitalis of a recessed region.

[Claim 12] The solar cell circuit according to claim 11 where the substrate concerned furthermore went caudad including a substrate, and a recessed region is extended.

[Claim 13] The solar cell circuit according to claim 11 which furthermore contains the second

diode section.

[Claim 14]The solar cell circuit according to claim 11 where formation of a recessed region makes a fall of an effective cell area less than 1%.

[Claim 15]The solar cell circuit according to claim 10 whose first conductor is a monolithic conductor.

[Claim 16]The solar cell circuit according to claim 10 whose first conductor is discrete metal Inta connection.

[Claim 17]The solar cell circuit according to claim 10 whose first conductor is C clamp metal Inta connection.

[Claim 18]It is a solar cell device. : A GaAs system cell;

The first contact combined with said GaAs system cell;

Tunnel diode which overlays said at least a part of GaAs system cell;

A GaInP system cell which overlays said at least some of tunnel diodes;

A cap which overlays said at least a part of GaInP system cell;

The second contact that overlays said at least a part of cap;

An epitaxial growth by-pass diode which overlays said at least a part of cap;

The third contact combined with said by-pass diode;

The fourth contact combined with said by-pass diode;

The first conductor combined with said second contact and the third contact; it reaches. A solar cell device containing the second conductor that carries out coupling to said first contact and the fourth contact.

[Claim 19]It is a solar cell device. : The first cell;

The first contact by which coupling was carried out to said first cell;

The second cell that overlays said at least a part of first cell;

The second contact combined with said second cell;

An epitaxial growth diode which overlays said at least a part of second cell;

The first conductor that carries out coupling of said first contact and said by-pass diode electrically; it reaches. A solar cell device containing the second conductor that carries out coupling of said by-pass diode to said first contact electrically.

[Claim 20]It is the protected solar cell device. : It has the first cell part and at least one connection and at least one solar cell contact are included on a rear face of said first cell part.;

It has at least one by-pass diode portion which grew epitaxially into said first solar cell portion. ;

Said by-pass diode portion has at least one contact, and reaches. A solar cell device containing discrete INTAKONEKUTO \*\* which combines said diode contact for said solar cell.

[Claim 21]The solar cell device according to claim 20 which contains further a majority of other solar cell portions which are in-series or in parallel with said first solar cell portion, and are combined.

[Claim 22]it is a spacecraft -- it being the first solar cell used in order to supply electric power to a spacecraft, and, Said first solar cell A cap layer Contact formed on said cap layer An integral by-pass diode which overlays said at least a part of cap layer, That in which said by-pass diode has at least one contact It has the Inta connection which combines cap layer contact with said diode contact, In a row A spacecraft which is the second solar cell used for \*\* which supplies electric power to said spacecraft and by which said second solar cell is combined with said first solar cell.

[Claim 23]It is a solar cell assembly. : It is a means to transform solar cell energy into electric energy, and said means is a means for changing solar energy which has a series of cells.;

A means to receive contact which overlays said at least a part of means for changing solar energy;

Contact which overlays said at least a part of means for receiving contact;

A solar cell assembly with which it is a means to protect said means from a reverse bias state in order to change solar energy, and said safeguard is combined with said contact using a conducting means.

[Claim 24]it is how to manufacture a solar cell circuit -- process; which provides the first photo voltaic cell

A process of providing the second photo voltaic cell combined with said first photo voltaic cell;

A process of providing a cap layer combined with said second photo voltaic cell; it reaches. A method including a process of providing an integral by-pass diode combined with said cap layer.

[Claim 25]it is how to manufacture a protected solar cell circuit -- in order to form at least some multi-junction solar cells -- the first -- process; into which two or more layers are grown up in order to form a diode -- said first [ the ] -- two or more -- a layer -- at least -- in part -- the second -- process; into which two or more layers are grown up

A process of carrying out etching removal of at least a part of second two or more layers;

It is one process of a layer of providing the first contact in part at least, two or more for a start [ said ].;

One process of said second two or more layers of providing the second contact in part at least;

A way it is the process of combining said first contact with said second contact, and said diode is what operates as a by-pass diode.

[Claim 26]A way according to claim 25 a layer contains two or more at least one cap layers for a start [ said ].

[Claim 27]How according to claim 26 for said cap layer to be arranged for said first contact in part at least.

[Claim 28]A method according to claim 25 by which said first contact is combined with said second contact using an integral conductor.

[Claim 29]A method according to claim 25 by which said first contact is combined with said second contact using a discrete conductor (discrete conductor).

[Claim 30]it is the protected solar cell circuit -- substrate;

The first photo voltaic cell combined with said substrate;

The second photo voltaic cell combined with the first photo voltaic cell;

An epitaxial growth by-pass diode combined with said second photo voltaic cell;

That in which it is a recessed region with at least one wall specified at least by said first photo voltaic cell, said second photo voltaic cell, and said diode, and said field is extended from said diode even to said substrate;

An insulator deposited on at least one wall of said recessed region;

A solar cell circuit containing an electrical conducting material which at least and said insulator deposited in part at least so that said diode and said substrate might be combined electrically. [ said diode ]

[Claim 31]it is a solar cell circuit -- first photoelectromotive-force partial;

A substrate; it reaches. A solar cell circuit containing a diode used in order to provide reverse bias protection formed between said first photoelectromotive-force portion and said substrate.

[Claim 32]The solar cell circuit according to claim 31 which furthermore contains the second photoelectromotive-force portion.

[Claim 33]The solar cell circuit according to claim 31 in which said first photoelectromotive-

force portion has P/N structure.

[Claim 34]The solar cell circuit according to claim 31 in which said by-pass diode has N/P structure.

[Claim 35]The solar cell circuit according to claim 31 in which said by-pass diode has P/N structure.

[Claim 36]The solar cell circuit according to claim 31 in which said first photoelectromotive-force portion has N/P structure.

[Claim 37]it is the Inta connection method of a solar cell : process; which carries out Inta connection of the first contact of the first solar cell that has an integral by-pass diode with the first contact of the second solar cell -- and -- The second contact of the second solar cell for the first contact of the first solar cell. A method including a process of carrying out Inta connection.

[Claim 38]A method according to claim 37 in which the first contact of said first solar cell carries out Inta connection with the second contact of the second solar cell using z-Tab Inta connection.

[Claim 39]A method according to claim 37 by which an interval is opened from said first contact [ in / in an integral diode of said first solar cell / the first direction ].

[Claim 40]It is the Inta connection method of a solar cell, A method including a process of carrying out Inta connection of the first contact of process; and the second solar cell that carries out Inta connection of the first contact of the first solar cell that has an integral by-pass diode with the first contact of the second solar cell at the second contact of the second solar cell.

[Claim 41]A method according to claim 40 in which the first contact of said second solar cell carries out Inta connection with the second contact of the second solar cell using a C clamp.

[Claim 42]A method according to claim 40 which has the first contact of said first cell in the surface of the first cell, and has the first contact of said second cell in the surface of the second cell, and has the second contact of said second cell in a rear face of said second cell.

[Claim 43]it is the Inta connection method of a solar cell -- process; which attaches a conductor to the first contact arranged on the surface of the first solar cell that has an integral by-pass diode -- and -- A method including a process of attaching a conductor to the second contact arranged on the surface of the second solar cell.

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## DETAILED DESCRIPTION

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[Detailed Description of the Invention]

Field this invention of a background invention of an invention relates to a solar cell. Especially this invention is an integral diode. (integral diode) It is related with the method and device for providing the solar cell which it has.

[0001]

The optical (photoelectromotive force) cell called a solar cell to the general indication target of a pertinent art is well known as a device which transforms solar energy into electric energy. In the object for the grounds, and the application to the both sides for the universes, the solar cell is used for years, in order to make electric power. For example, a solar cell provides a clean power generation means. It is not necessary to fill up a solar cell with a fossil fuel. Instead of it, the solar cell operates by the energy infinite as a matter of fact of the sun. However, since a solar cell

is a comparatively expensive power generation method, use of a solar cell is limited. Nevertheless, in the universe from which a convenient energy source is not acquired by low cost, a solar cell is an attractive device for an energy manufacturing method.

[0002]

A solar cell is generally assembled by the solar cell array connected by the combination of series, parallel, or a serial parallel. As for desired output voltage and current, at least a part determines the number of cells in an array with array TOPOROGI (array topology).

[0003]

If the optical exposure of all the cells in an array is carried out as known for the field concerned, each cell will serve as forward bias. however, 1 or the cell beyond it carries out optical interception with a satellite antenna etc. -- having (an optical exposure will not be carried out) -- the cell by which optical interception was carried out serves as reverse bias with the voltage produced by the cell by which optical interception was carried out. The reverse bias of a cell causes an eternal fall or the perfect cell defect of the capability of a cell. Usually \*\* also provides a \*\* sake with a protection by-pass diode for a cell from these damages. In order for one by-pass diode to cross some cells, and to connect it and to improve reliability, each cell can also have a self by-pass diode. A multi-junction solar cell tends to receive a damage especially under reverse bias conditions. For this reason, especially the multi-junction solar cell can receive profits from one by-pass diode per cell. In the former, a by-pass diode is connected by contrary parallel arrangement (anti-parallel configuration), Since the anode and cathode of a by-pass diode are connected to the cathode and anode of a solar cell, respectively, a by-pass diode serves as reverse bias, when the optical exposure of the cell is carried out. Most current flows through a by-pass diode rather than the cell by which optical interception was carried out, and, thereby, current continues flowing in an array. In addition, a by-pass diode restricts the reverse bias voltage which crosses the cell by which optical interception was carried out, and the cell by which optical interception was carried out by this is protected.

[0004]

Some different conventional methods are used in order to supply the solar cell by by-pass diode protection. Any conventional method has a fault. For example, in order to try grant of the increased bypass protection, one method includes connecting the anode of a by-pass diode to one cell, connecting the cathode to the next cell, and arranging a by-pass diode between the cells which adjoined. However, in this art, a cell is assembled by the array, before by-pass diode protection is given. This assembly method is difficult and is inefficient-like. and in this art, it rubs by a cell manufacturer -- carry out -- the by-pass diode which should be given by the array assembly contractor is needed. In addition, in this art, the cell which can take the space enough left so that it could be adapted in a by-pass diode is called for. By this space reservation, it becomes an array of a low packing factor and, thereby, an array will become inefficient to an area base.

[0005]

It is necessary to form RESESU or a crevice (recess) behind [ that a by-pass diode is arranged ] a cell in other conventional technologies which provide each cell with a by-pass diode. The first polarity contact (first polarity contact) on the surface of a cell is given to each cell, and the second polarity contact is supplied to it on the rear face of each cell. Smooth S form Inta connection is joined to surface contact of the cell which adjoins from rear-face contact of the first cell after that. Thus, in order to adapt the Inta connection which must pass by this art along between the adjoining cells, the cell from which the interval which separated enough was

secured is required, and it is disadvantageous. The further fault of this method is that there is a possibility that a micro crack may arise in the formation stage of a crevice. In addition, in this method, since the thick bond line for adhesion is required, stress rise ZASU (stress-risers) is given and the stress generated between temperature cycles increases. In this conventional technology, connection of the Inta connection of the adjacent cell which should be carried out by the array assembly contractor is reversely required as a cell manufacturer.

[0006]

One concrete mode of abstract this invention of an invention provides advantageously the method and device for providing the integral by-pass diode of a solar cell efficiently. The solar cell of one mode is a multi-junction cell. A by-pass diode is grown up into a MONORISHI curry at at least some solar cells. As for other modes, a solar cell is formed from the material of III, IV, or V fellows at least. As a mode of further others, a diode contains N-type GaAs layer and a P-type GasAs layer at least. As a mode of further others, a diode is formed using material with germanium or a comparatively low band gap like InGaAs.

[0007]

As for one concrete mode, a solar cell contains a germanium germanium substrate. germanium substrate may also include photoactive connection further. being the further -- others -- a semiconductor [ like / a substrate / :GeAs and Si which are formed from at least one sort of the following material, or InP ] whose mode is, and an insulator like sapphire. In one mode, a substrate is a single crystal.

[0008]

As for other modes, C-clamp conductor does Inta connection of at least one solar cell contact at at least one by-pass diode contact. Other modes carry out Inta connection of at least one of the by-pass diode contacts for at least one of the solar cell contacts using the Integra RIMETARAIZUDO layer (integrally metallized layer). The mode of further others makes the Integra RIMETARAIZUDO layer deposit on an insulating layer, and prevents the Integra RIMETARAIZUDO layer short-circuiting in other layers beyond 1 or it.

[0009]

As for one mode, a cap layer carries out Inta connection of the first diode pole (first diode polarity) at a solar cell. In the mode of further others, a by-pass diode is grown epitaxially on a solar cell with 1 or connection beyond it. :GaAs, InP, GaInP<sub>2</sub>, and AlGaAs in which a solar cell may be formed in the mode of further others from more than at least one sort or it of the following material. In another mode, in order that other III-V compounds may form at least some solar cells, it is used.

[0010]

These modes in this invention and other features, an effect, and the new feature are clarified with a specification and the following accompanying drawing.

[0011]

Detailed explanation this invention of a desirable embodiment is at least one integral by-pass diode. (integral bypass diode) It is related with the solar cell which it has. A solar cell may be single junction (single junction) or two or more junction (multijunction) cell. As shown below, a by-pass diode is grown epitaxially on a multi-junction solar cell as one mode. Inta connection is carried out with other solar cells, and a solar cell / by-pass diode device forms the in-series and/or parallel string (strings) of a solar cell. The healthy solar cell array which connects each string further and is reliable may be formed. A solar cell array may be installed in a space vehicle or a spacecraft (space vehicle), and, thereby, supplies power or electric power to a space vehicle

or a spacecraft.

[0012]

In one mode of this invention for forming the multi-junction solar cell 100, drawing 1 shows an order of III-V \*\*\*\*\* 106-122 continuously grown up on the germanium substrate 102. The germanium substrate 102 may also include photoactive junction (photoactive junction) further. In one mode, although each class is grown epitaxially, when this reproduces the single crystal structure of material, it is meaningful. A growing parameter (deposition temperatures, a growth rate, compound alloy composition, concentration of impurity dopant) can be optimized preferably, the layer which has desired electric nature and thickness can be provided, and the overall cell performance demanded by this can be obtained. The epitaxial technique used in order to grow up a cell layer, For example, MOCVD (metal-organic chemical vapor deposition) epitaxy, What is called OMVPE (organic-metallic vapor phase epitaxy), MBE (molecular beam epitaxy) and MOMBE (metal-organic molecular beam epitaxy) are included.

[0013]

In the illustrated mode, N dope GaAs base layer 106 is grown up, and at least some substrates 102 are overlaid. Photoactive junction is formed in the contact surface of the layer 102 and the layer 106. In one mode, photoactive junction is a N+GaAs/N+germanium hetero diode. As other modes, in growing up N/P composition, the P type germanium substrate 102 is used and diffusion of As from the layer 106 forms N/P junction in the substrate 102.

[0014]

As shown in drawing 1, the GeAs base layer 106 grows up the high P dope (highly Pdoped) GaAs emitter layer 108 in part at least. The base layer 106 and an emitter layer (108) form a both more low cell stage (a lower cell stage). The high P dope AlGaAs window layer 110 is overlaid on the emitter layer 108. The tunnel diode which contains the quantity dope P (very highly P doped) and the N layers 112 and 114 very much is grown up on the window layer 110. The second or the more nearly upper cell stage containing N dope base layer 116 and the high P dope emitter layer 118 is made to form on tunnel diode.

[0015]

As one mode, two layers of the last of a solar cell are the high P dope AlGaAs window 120 and the GaAs cap layer 122, respectively.

Said high P dope AlGaAs window 120 is a thin hyaline layer, and passivates the surface of the emitter layer 118 of a top cell ( $\text{GaInP}_2$ ) (carrier recombination is controlled), and surface ohm contact deposits said GaAs cap layer 122.

As one mode, in order to balance low electrical resistance and high optical transparence, grid finger formation (grid-finger form) has contact. However, other contact patterns may be used. In this mode, as shown below, an integral by-pass diode is included by the mono- RISHIKARU growth cellular structure (monolithically-grown cell structure) by growth of some additional layers. It is selectively removed between grid lines and the cap layer 122 is antireflection coating. (anti-reflective coatings) It deposits on the top window layer 120.

[0016]

The 3 cell 3 junction solar cell 100 shown in drawing 1 is one of a majority of possible cell modes which can be used in this invention so that a person skilled in the art can understand. In other modes, complementarity structure (complementary structure) with converted 1 or the polarity beyond it (for example, P dope of N doped layer is done as a substitute, and P dope of P doped layer is done as a substitute) can be used. For example, the composition of the cell and diode which are shown in a figure and explained below can be changed into N/P from P/N.

Doping concentration or layer thickness is also various. The solar cell 100 is the photo voltaic cell or photoelectric conversion cell beyond four or it as other modes. (photovoltaic cell) It may contain or 1 or two cells may be included. Similarly, one junction, two, or junction beyond it may not be in a solar cell, but it may also contain \*\*. According to an example, the cell 100 may include four junction as one mode.

[0017]

The solar cell 100 may contain the cell which consists of other materials like AlGaAs or InP. As other modes, the substrate 102 may construct a different material and may carry out \*\*\*\*\* formation. For example, other semiconductors like GaAs, Si, or InP may be used for the solar cell 100 as a substrate rather than germanium substrate shown by drawing 1. An insulating base material like sapphire may be used. As one mode, the substrate 102 is a single crystal. As for cell materials, when the solar cell 100 is planned for [ like a spacecraft or a satellite ] the universes, it is preferred to be optimized for the universes for the suitable space environment (space-qualified). For example, the solar cell 100 and the by-pass diode may be optimized for the universes so that it may operate under an AMO radiation environment.

[0018]

One method of manufacturing a by-pass diode is explained. As shown in drawing 2, the by-pass diode 212 is contained in the solar battery structure using the five added growth phases 202, 204, 206, 208, and 210.

[0019]

As stated also in advance, the layer 106-122 containing the photoelectromotive-force portion of a multi-junction solar cell is first grown up as one mode, the growth cycle is continued and the additional layer 202-210 is grown up. From the P type GaAs cap layer 122 used for surface grid contact. An additional layer is in order. : High dope N-GaAs connecting layer 202 used in order to lower the contact resistance to - N-GaAs diode layer 206 and the high dope GaAs cap layer 122.

[0020]

- The stop dirty layer (stop-etch layer) 204 (high N dopes AlGaAs and GaInP) used in order to perform etching removal by which the three diode layers 206-210 were controlled.

[0021]

- N dope GaAs layer 206 which consists of a negative dope portion of the by-pass diode 212.

[0022]

- P dope GaAs layer 208 which consists of a positive dope portion of the by-pass diode 212.

[0023]

- The high dope P-GaAs layer (210) which supplies good metallic contact to P layer of a diode (212)

However, in other modes of this invention, a different number of layers formed from the material of a different type which has a different dopant from the above-mentioned mode may be used so that a person skilled in the art may also understand. For example, N/P can consist of a N/P multi-junction solar cell and a N/P by-pass diode from use of complementarity structure, i.e., P/N, in a similar manner rather. The diode 212 may be formed using germanium or low band gap material (lower bandgap materials) like InGaAs. As other modes, it may leave the layer 204 which provides stop etching and electric conduction, and the layer 202 may be omitted.

[0024]

One of the manufacturing methods of the wafer which forms one mode of this invention is explained after this. DEFAIN according [ a manufacturing process ] to growth and the mesa etch



(mesa etch) in the mode of this invention (define) And it is used in order to carry out Intra connection of the one mode of the by-pass diode 212 at the cascade (multi-multi-junction junction) cell 100.

[0025]

First, the photoactive solar battery layer and diode layer which are shown in drawing 2 are grown epitaxially using conventional MOCVD and/or MBE art. As shown in drawing 3, a series of surfaces or front faces (front surface) of a growth phase are exposed through the photo mask (not shown) by which the pattern was carried out, in order to leave the diode layer which was protected by the photoresist layer 302 and covered with resist. As shown in drawing 4, the diode cap layer 210, N, and P diode layers 206 and 208 are etched to the stop dirty layer 204. Etching may be carried out using the citrate heated by 45 °C. As shown in drawing 5, the stop dirty layer 204 removes the portion by which a mask is not carried out by the photoresist layer 302, and the suitable portion of the N dope GaAs connecting layer 202 is exposed. When the stop dirty layer 204 is AlGaAs, an etching reagent may be BHF (buffer hydrogen fluoride) acid as one mode. When the stop dirty layer 204 is GaInP, an etching reagent may be HCL as other modes. As shown in drawing 6, the photoresist layer 302 is removed using acetone. Micro stripe art (microstripping techniques) can also be used in order to remove the remains photoresist portion which remains after an acetone removal process.

[0026]

Once it removes the photoresist layer 302, the front contact manufacturing process containing corresponding photoresist coating, baking, exposure, developing, metal deposition, and lift-off OPERATION will be performed. The coat of other photoresist layers (not shown) is carried out to the whole surface. A photoresist layer is burned and exposed to a front grid line and a pad, N dope GaAs layer 202 small region, and a diode cap layer using the photo mask which leaves the open area which is a portion which contact deposits. The metal which contains Ag as the main ingredients is vapor-deposited all over an exposed region and on the remaining photoresist layer. In addition to the two contact regions 702 and 704 as shown in drawing 7, photoresist also supplies an open slot into photoresist and supplies a grid line and a bar / pad contact to a cell. Next, a lift-off process is carried out. The solar cell slice 100 is immersed in acetone, swells photoresist, and pulls down all the metallic films other than the field specified in order for this to maintain contacts including the contacts 702 and 704.

[0027]

As shown in drawing 8, the metal which uses Ag as the main ingredients is vapor-deposited by the rear face of germanium substrate, and forms the rear-face metallic contacts 802. The contacts 702, 704, and 802 are heat-treated or sintered after that. Using the front contact metals 702 and 704 as a dirty mask, as the GaAs cap layer 122 is shown in drawing 9, the great portion of exposed surface is etched. The cap layer 122 remains under the metalized field, and forms a low resistance contact mechanism portion.

[0028]

As shown in drawing 10, the diode pad metallic contacts 702 and 704 and the small contact shown in the surroundings of the diode 212 are protected by a resist mask, and the antireflection layer (anti-reflecting layer) 1002 deposits it on the surface of the remainder. As shown in drawing 11, the top, P side, and the diode contact 702 are connected to the rear-face cell (N-grid) contact 802 by combining the thin Intra connection 1102. Thus, in one mode, the electrical link between the P-layer 208 of the P/N GaAs diode 212 and the back side of an N dope germanium substrate is formed of C clamp 1102 connected with both the surface diode contact 702 and the

rear germanium contact 802. Thus, the by-pass diode 212 crosses the both sides of a photo voltaic cell, and is connected. In other modes, a by-pass diode is used in order to bypass 1 or the photo voltaic cell beyond it. Thus, in one mode of this invention, it can use in order to bypass cells of all [ or ] fewer than it in the solar battery structure 100.

[0029]

A solar cell can be used for the mode of other Inta connection art in order to connect a by-pass diode. Final selection is based on the influence which it has on the cell quantity of production and cost which are brought about from the complexity added and these alternative approaches. For example, some other explanation is shown below.

[0030]

As shown in drawing 12, in one mode Diode top contact, In order to expose germanium substrate, one short contact between the metalization fields on the small trough (small trough) etched through the cascade cell layer 1206-1218 can be used rather than a C clamp. A trough is an effective cell area. (active cell area) Less than 1% may be removed and it may arrange near the top contact of a by-pass diode. In a previous mode, the mode shown in drawing 12 shows the front metallic contacts 1224, the rear-face metallic contacts 1202, and the antireflection coating 1226. Some different contact gestalten can be used. for example : a -- as one mode (not shown), it is connected with diode contact by an end, and direct continuation of the short dispersion metal Inta connection (short discrete metal interconnect) is carried out to germanium surface exposed all over the trough. Preferably, the Inta connection is gold-plated. It can be used in order that various art may build combination. In one mode, combination is performed using eutectic Au-germanium soldering.

[0031]

b) In (a), in difficulty or the case which is not preferred, the direct continuation on the surface of germanium can also add a process additional as other modes in the usual cell process. Except for the place for which germanium contact region is needed using a dry film or fluid photoresist, the mask of the surface (front surface) is substantially carried out to all the fields. Then, in order to form a grid, an ohm, and diode contact, when surface metallic contacts accumulate through other photoresist masks, the edge of a trough can be protected by resist by using the vacant field in an etched field. The metal for contacting N-germanium may be vapor-deposited in a series of vacuum evaporation which is the same as the case where front contact of the cascade cell 100 and the diode contacts 702 and 704 are formed, or is similar. In this case, TiAuAg or equivalent contact is given to the exposed region on a front face.

[0032]

c) As shown in drawing 12, in perfect monolithic structure (fully monothilic structure), a trough or a crevice (recess) is etched even to the germanium interface 1204 through a diode and the cell layer 1206-1218. Thus, the wall or wall group of a trough is formed of a cell layer. Since a mask exposes the edge of a trough, it is used after that, and the insulating layer 1220 is deposited on the field between layer edge and the diode cap layer 1218, and a trough. Since the metal 122 which connects front contact of a diode is deposited on the trough which exposes the germanium substrate 1204, other masks contained in a main front contact mask are used. In other modes, diode contact is not required for the substrate-diode INTA connection 1222.

[0033]

The perspective view of one mode of the solar cell 100 including the by-pass diode circuit 212 is shown in drawing 13. The front face of the solar cell 100 contains the grid line 1302 by which Inta connection was carried out with the ohm bar 1306. The above-mentioned bar 1306 is

fabricated so that the field or crevice in which the diode 212 is formed may be provided. In one mode, Intra connection of the diode 212 is carried out at the rear-face contact 802 of the solar cell 100 using the C clamp connector 1102 shown by drawing 11. Drawing 13 B is an enlarged detail of the by-pass diode 212 shown by drawing 13 A. one mode -- both the sides of the diode 212 -- the ohm bar 1306 and \*\*\*\*\* -- it is. Thus, the distance of the diode 212 and the bar 1306 becomes short. More bars 1306 are approaching the diode 212.

[0034]

As drawing 13 A shows, in order to connect with an adjoining assembly, the three tabs 1304 are formed in one mode. The tab 1304 may contain U type stress mitigation portion (U-shaped stress relief section) and what is called a Z tab. The first Said Intra connection of each tab 1304 is connected to the anode of the cell 100. Intra connection of the solar cell 100 may be carried out at the second solar cell by connecting the second side of the tab 1304 to the cathode of the second solar cell. In one mode, the tab may be formed from a silver and silver-invar (silver-invar) or silver-clad MORI (silver-clad moly) material.

[0035]

A cover glass (not shown) may be used in order to protect a solar cell or a by-pass diode device. A cover glass may become the universes from the borosilicic acid cover glass by which the Seria dope was carried out. In one mode, the cover glass is 50 micrometers to about 200 micrometers in thickness. The cover glass by which the Seria dope was carried out gives the radioactivity-proof which covers a charged particle or an uncharged particle. In one mode, when exposed to AMO cosmic radiation environmental spectrum (AMO space radiation environment spectrum) (spectrum discovered in the solar surrounding earth orbit out of earth atmosphere), a cover glass, Transparency is maintained substantially. The main effects in one mode of an integral by-pass diode do not need a notch or the use of a cover glass by which the slot was carried out, in order not to extend a diode on the surface of the solar cell 100, therefore to apply an integral diode. However, in one mode, a yne DEKURARU diode may be lengthened on the front face of the solar cell 100, or the top surface. If it is a person skilled in the art, it can be understood that other suitable cover glass materials and shape are employable similarly.

[0036]

Drawing 14 A shows other modes of this invention further. The illustrated solar cell 1400 contains the new embedding protection by-pass diode (buried protective bypass diode) 1410. Like the by-pass diode 212, the protection by-pass diode 1410 is used in order to protect a solar cell from the reverse bias state produced by the light shield of a cell.

[0037]

A series of typical growth phases shown in drawing 14 A are similar to it of drawing 1 A. The two added embedding layers 1406 and 1408 are provided in order to give the polarity which suits the germanium+ emitter 1404. The solar cell 1400 contains germanium substrate with which germanium emitter layer grew on it. The isolated diode layer 1412-1420 forms a by-pass diode function part. The layers 1422 and 1424 form the usual top cell, and the window layer 1426 and the cap layer 1428 are on it. In other modes, complementarity structure with 1 or the polarity beyond it changed from what was shown by drawing 14 A (for example, thing by which N dope of P doped layer was instead done, and P dope of N doped layer was done instead) can be used.

[0038]

A solar cell is manufactured like the above, and as shown in drawing 14 B, the rear-face metallic contacts 1430 and the surface metal diode contact 1440 are formed. In addition, the antireflection coating 1432 is applied.

[0039]

In one mode, the short integral connector 1436 is formed on the insulator 1434 from the cap layer 1428 on the small trough 1438 etched to the tunnel diode layer 1408 through the cell layer 1420-1412. In a connection like C clamp 1442 can be used in order to connect the rear-face metallic contacts 1430 and the front metallic contacts 1440. Thus, the by-pass diode 1410, It is connected with an antiparallel gestalt (anti-parallel configuration) about the photoelectromotive-force portion of the solar cell 1400, and since this provides the reverse bias protection to the photoelectromotive-force portion of the solar cell 1400, it is arranged.

[0040]

by using the above art partly at least, especially as for the solar cell with which the integral diode formed on the cascade cell was incorporated, the efficiency of not less than 23.5% was attained not less than 21%. Such efficiency is equal to general-purpose KASHIKEDOSERU which does not have an integral by-pass diode. In one mode, an integral by-pass diode has about 1.4-1.8-volt forward bias voltage descent at the time of energization of 400-mA forward current. Reverse breakdown voltage is enough to block the current passed to a by-pass diode between the usual non-light interception and illuminations, when a solar cell is forward bias. In one mode, reverse breakdown voltage is larger than 2.5V.

[0041]

In the example of the mode of this invention, with the cell area of about 24-cm<sup>2</sup>, there is also no remarkable performance change and the repetition 10-second pulse of a 400-mA reverse current was able to be maintained. Thus, when 2500 pulses were presented with one batch or lot of a solar cell in which 1 \*\*\*\*\* of the integral diode was incorporated by a 400-mA reverse current for example, the following performance changes were accepted.

Parameter Measured value before an examination Measured value VOC 2474mV 2476mV  
before an examination (open circuit voltage)

ISC 360.5mA 359.0mA (short circuit voltage)

CFE 81.5% 81.5% (curvilinear factor)

Efficiency 22.1% 22% By other examinations, when the reverse current of bigger

MAGUNECHUDO than ISC passed the solar cell 100, diode adjacent spaces showed a 10-12 \*\* rise in heat. This small rise in heat does not serve as a big adverse effect on the photoelectromotive-force portion of a cell, and the performance of an integral diode.

[0042]

In other desirable modes, as mentioned above, change of the \*\* sake of the further promotion is made so that the design of a solar cell can be used for all of the concentrator system for a space base or ground bases. It is necessary to protect from optical interception of the solar cell by clouds, the bird, the building, the antenna, and other structures like the case in a non concentrator system exactly. Thus, a protective diode is used in order to protect a solar cell from the reverse biased state by optical interception. However, the solar cell in a concentrator collects typically quite bigger electric power than a non concentrator solar cell. Thus, the capability to radiate the heat accompanying big electric power is needed rather than a protective diode is bypassed.

[0043]

In one mode, the crossing distribution demultiplexing bypass integral diode (distributing multiple separated bypass integral diodes) contributes at least a part of surface of a solar cell to heat leakage. Thus, a multiplex integral diode radiates a part of heat which bypassed a part of reverse bias electric power, and was corresponded and produced. Thus, the single integral diode needs to bypass no reverse bias electric power, or needs to radiate no heat accompanying such a bypass

function. A multi-integral by-pass diode may be formed using the same art as the above-mentioned art which forms one integral diode. In one mode, in order that a different photo mask may form a diode and diode contact, it is used.

[0044]

Drawing 15 A shows how to be in-series and carry out Inta connection of the solar cell with an integral by-pass diode. For example, the two solar cells 1502 and 1510 have the corresponding integral by-pass diodes 1504 and 1514, and Inta connection is carried out and they form the solar cell string 1500. The front contact 1506 with which the first Inta connection 1508 overlays the cascade cell of the solar cell 1502, By connecting with the front contact 1512 which overlays the yne DEKURARU by-pass diode of the solar cell 1510, the solar cells 1502 and 1510 are combined electrically. A jumper bar, a wire, etc. may be sufficient as the first Inta connection 1508. the second Inta connection 1518 -- the front contact 1506 of the solar cell 1502, and the tapir of the solar cell 1510 -- it is connected to the contact 1516. z-tab, a wire, etc. may be sufficient as the second Inta connection 1518. In the illustrated mode, the by-pass diodes 1504 and 1514 are suitably installed in the edge or side of an opposite hand of the ohm Celcon baton pads 1506 and 1520.

[0045]

Drawing 15 B is in-series to a solar cell with an integral by-pass diode, and shows other methods of carrying out Inta connection to it. The first Inta connection 1508 is connected to the front contact 1506 of the solar cell 1502, and the front contact 1512 of the solar cell 1510 like a precedent. The second Inta connection 1518 is connected to the front contact 1512 and the pack contact 1516 of the solar cell 1510. A C clamp, a wire, etc. may be sufficient as the second Inta connection 1518. As for this mode, it is preferred to use one Inta connection between two adjoining cells, and the series connection between cells is formed on the surface of a cell. Thus, for example, a cell has the correspondence C clamp individually attached in the first place by the battery manufacturing contractor. A solar panel assembly machine carries out Inta connection at front contact of a cell which was illustrated to drawing 15 B. Efficient, high yield manufacture of a solar cell, a cell string, and a solar panel are provided with this method.

[0046]

Although the desirable mode of this invention is indicated, these are mere illustration and limiting the range of this invention is not shown.

[Brief Description of the Drawings]

[Drawing 1]

Drawing 1 shows the first manufacturing process used in order to assemble one mode of this invention.

[Drawing 2]

Drawing 2 shows the second manufacturing process used in order to assemble one mode of this invention.

[Drawing 3]

Drawing 3 shows the third manufacturing process used in order to assemble one mode of this invention.

[Drawing 4]

Drawing 4 shows the fourth manufacturing process used in order to assemble one mode of this invention.

[Drawing 5]

Drawing 5 shows the fifth manufacturing process used in order to assemble one mode of this

invention.

[Drawing 6]

Drawing 6 shows the sixth manufacturing process used in order to assemble one mode of this invention.

[Drawing 7]

Drawing 7 shows the seventh manufacturing process used in order to assemble one mode of this invention.

[Drawing 8]

Drawing 8 shows the eighth manufacturing process used in order to assemble one mode of this invention.

[Drawing 9]

Drawing 9 shows the ninth manufacturing process used in order to assemble one mode of this invention.

[Drawing 10]

Drawing 10 shows the tenth manufacturing process used in order to assemble one mode of this invention.

[Drawing 11]

Drawing 11 shows one mode of this invention including the discrete Inta connection.

[Drawing 12]

Drawing 12 shows one mode of this invention including integral INTA connection.

[Drawing 13]

Drawing 13 A is a perspective diagram of one mode of this invention.

Drawing 13 B shows the enlarged detail of the by-pass diode shown by drawing 13 A.

[Drawing 14]

Drawing 14 A shows one mode of this invention which has an embedding by-pass diode.

Drawing 14 B shows one mode of drawing 14 A after the further process was performed.

[Drawing 15]

Drawing 15 A shows the primary method which carries out Inta connection of the solar cell.

Drawing 15 B shows the second method of carrying out Inta connection of the solar cell.

## DRAWINGS

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[Drawing 1]

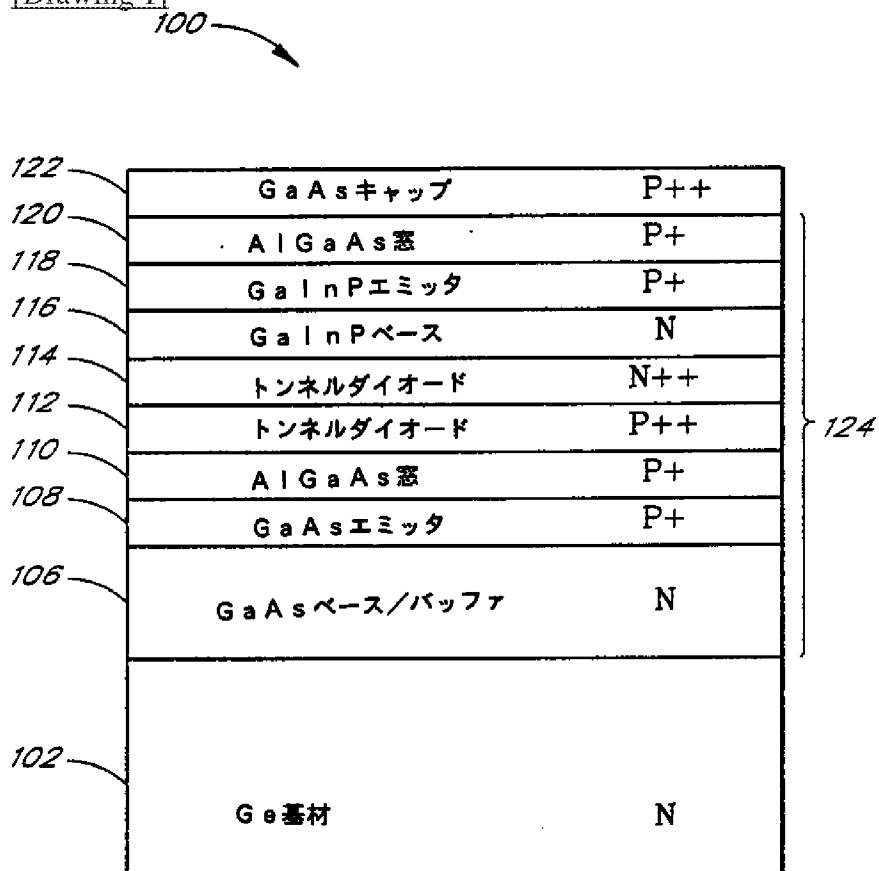


FIG. 1

[Drawing 2]

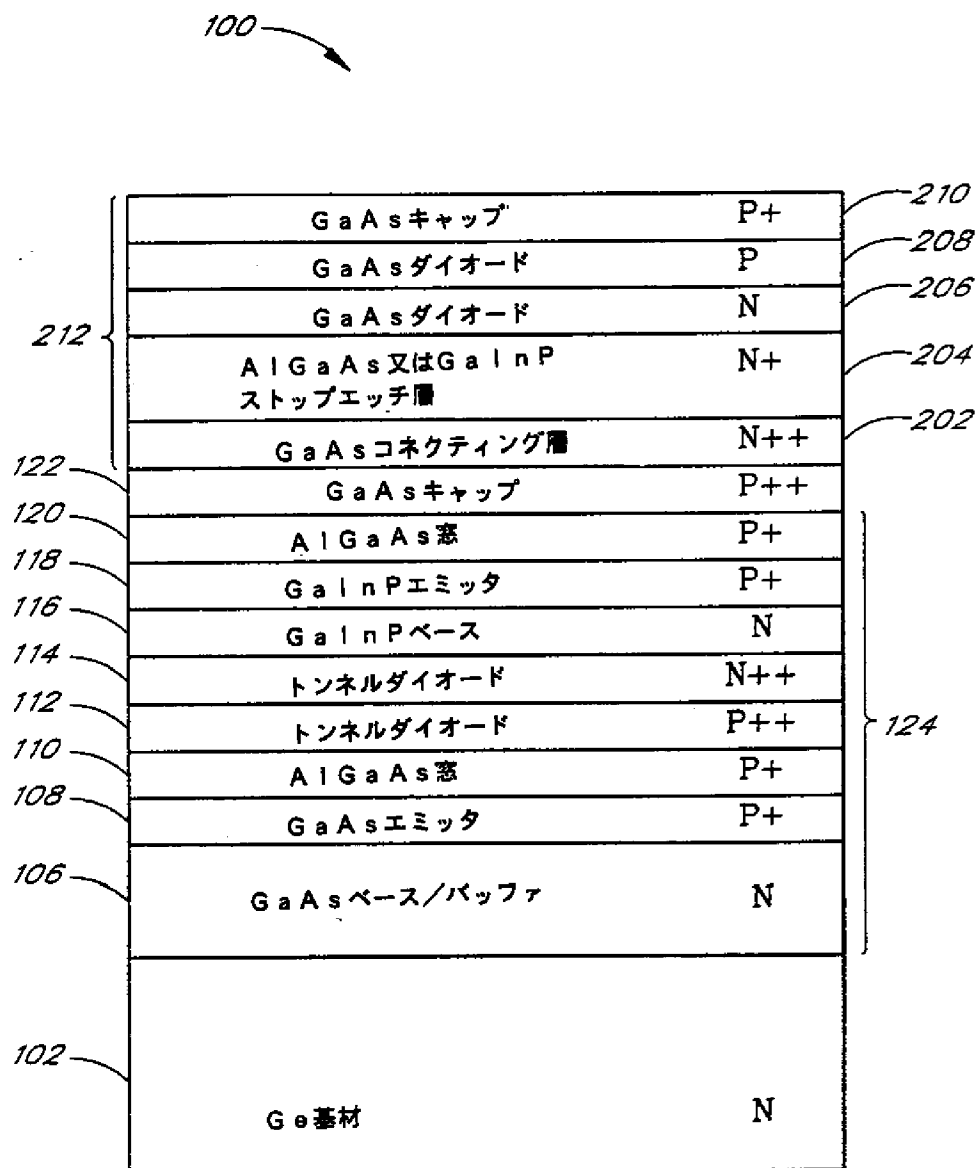


FIG. 2

[Drawing 3]



302	フォトレジスト層	
216	ダイオードキャップ層	P++
208	p-ダイオード層 (GaAs)	
206	n-ダイオード層 (GaAs)	
204	ストップエッチング層 (AlGaAs又はGaInP)	
202	GaAs Nコネクティング層	N++
122	GaAsキャップ層	P++
124	カスケード太陽電池 P/N	
102	Ge基材	N

FIG. 3

[Drawing 4]

クエン酸 (45°C, 1 min.)

フォトレジスト層	
ダイオードキャップ層	P++
p-ダイオード層 (GaAs)	
n-ダイオード層 (GaAs)	
ストップエッチング層 (AlGaAs又はGaInP)	
GaAsコネクティング層	N++
GaAsキャップ層	P++
カスケード太陽電池 P/N	
Ge基材	N

FIG. 4

[Drawing 5]

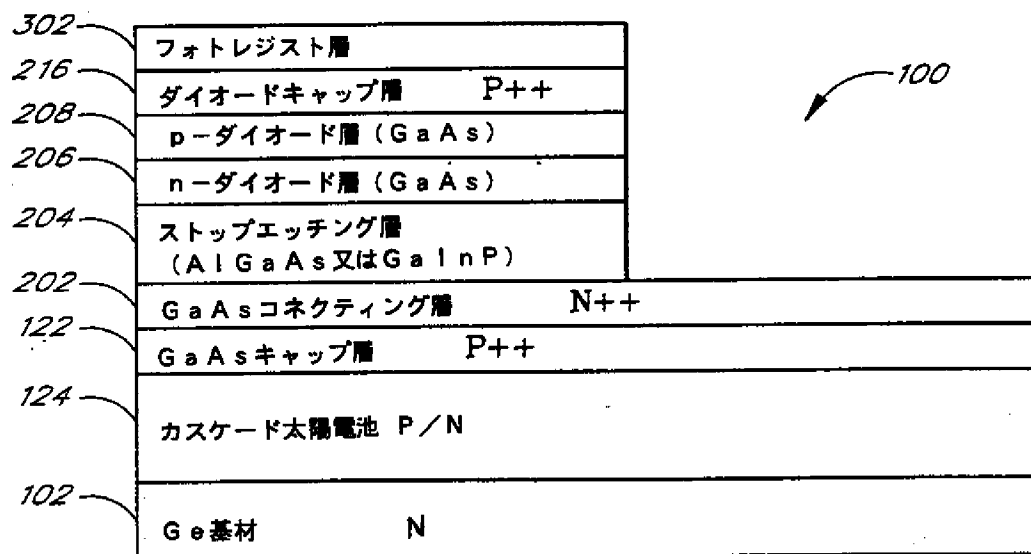


FIG. 5

[Drawing 6]

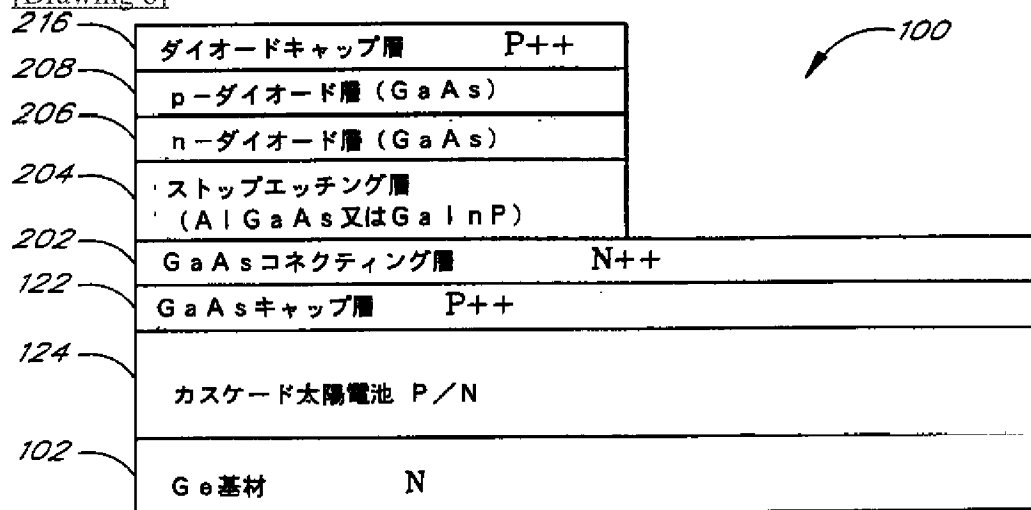


FIG. 6

[Drawing 7]

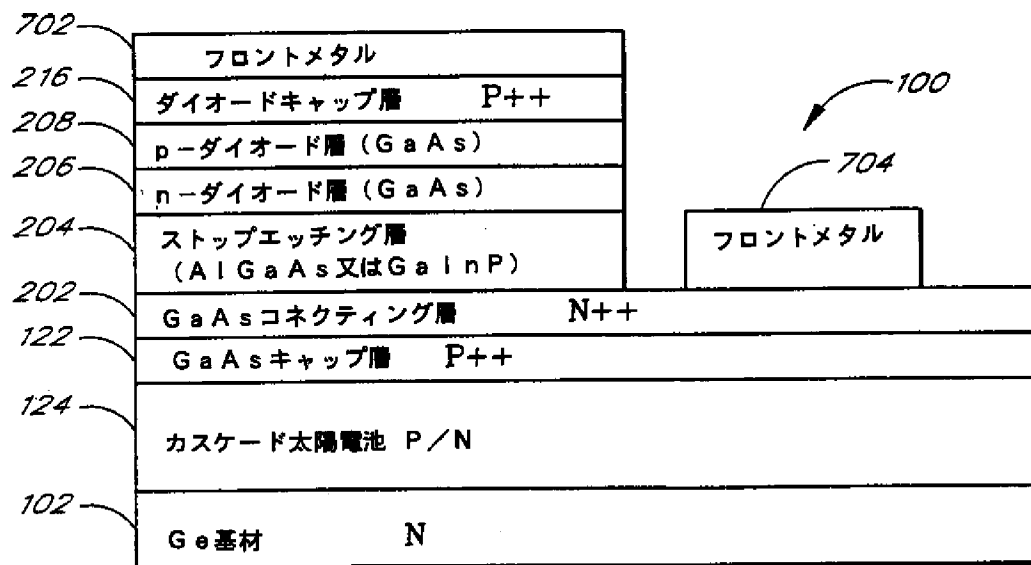


FIG. 7

[Drawing 8]

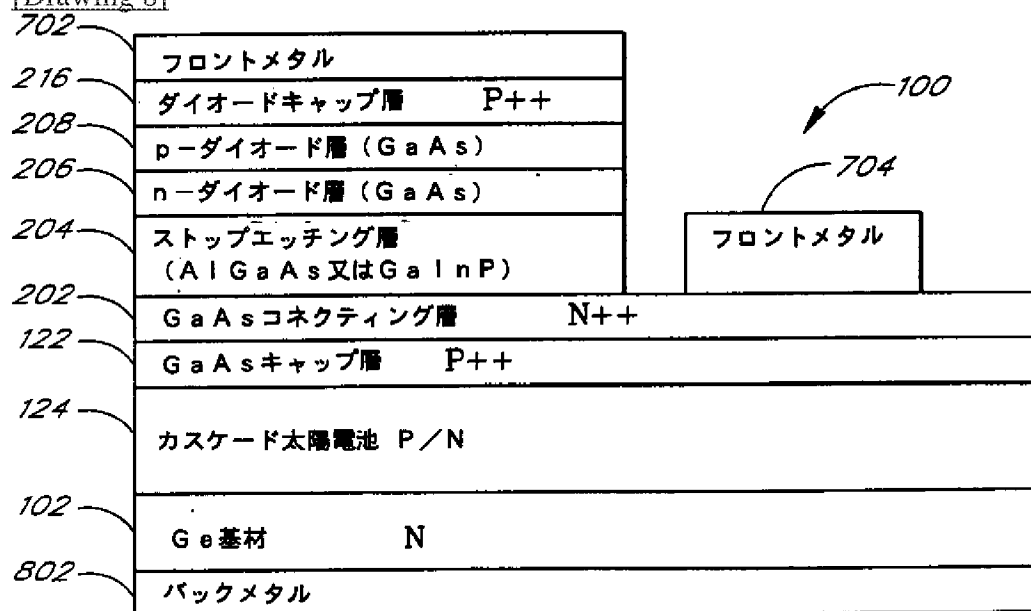


FIG. 8

[Drawing 9]

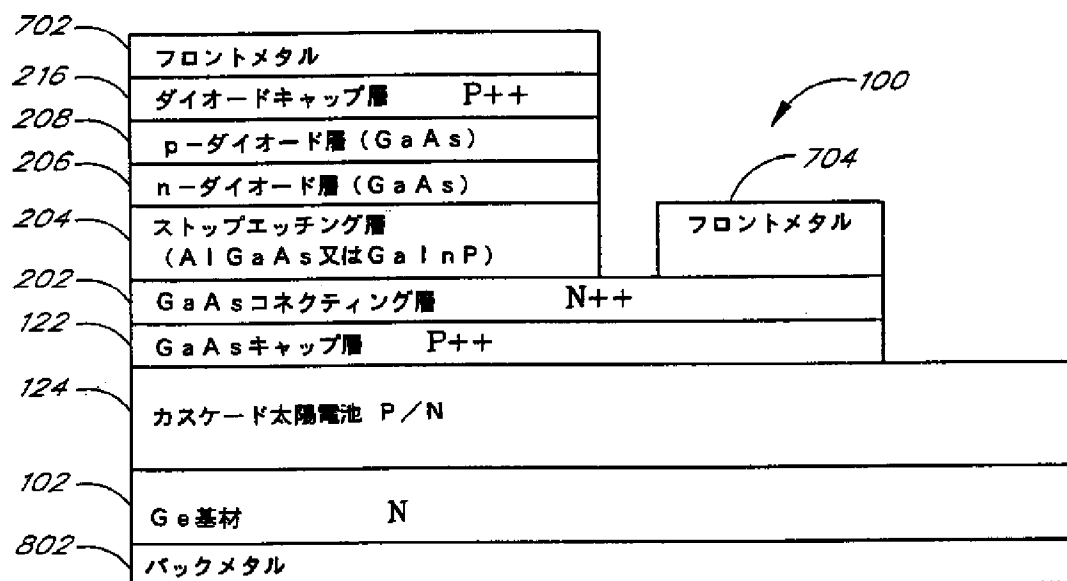


FIG. 9

[Drawing 10]

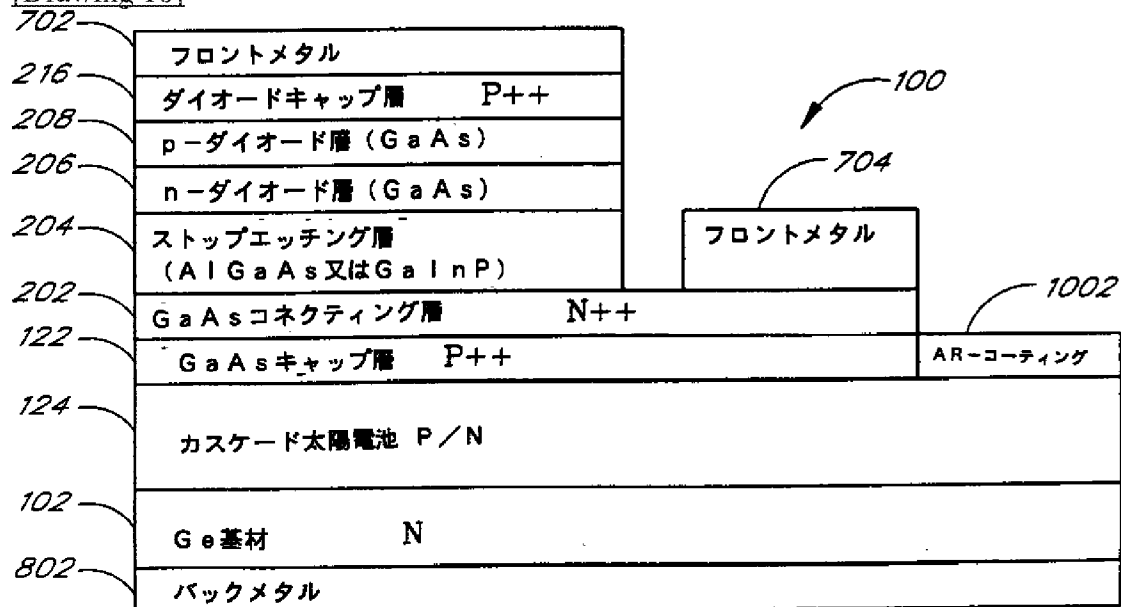


FIG. 10

[Drawing 11]

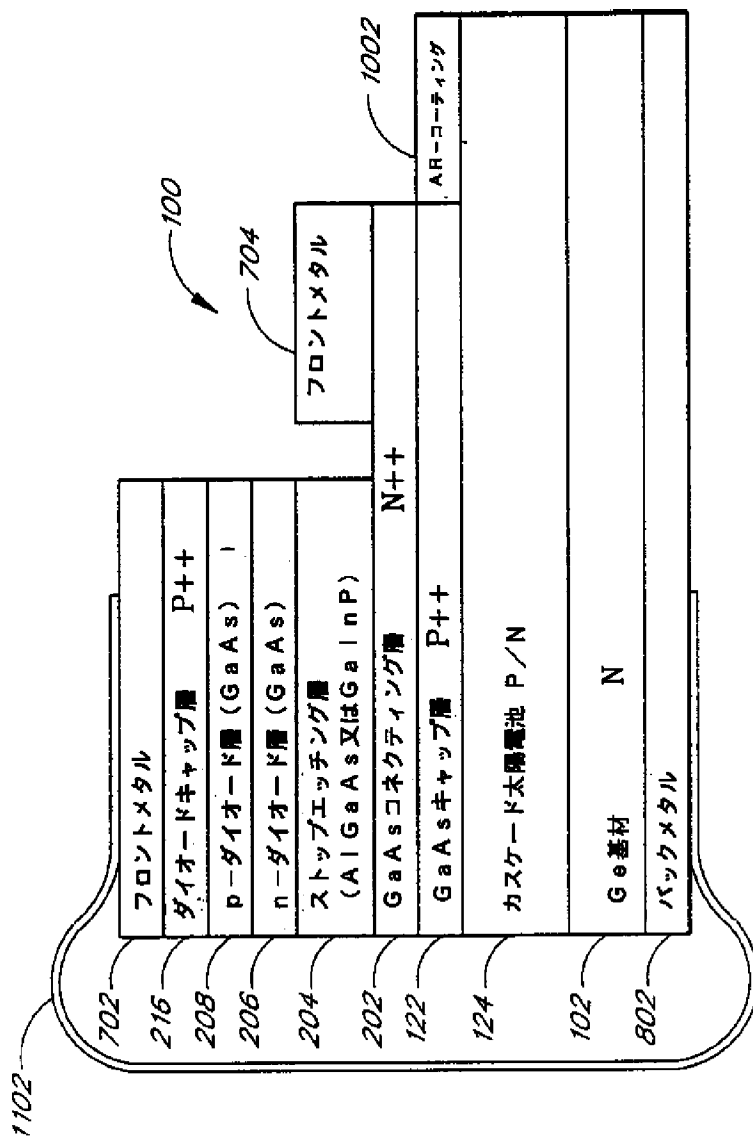
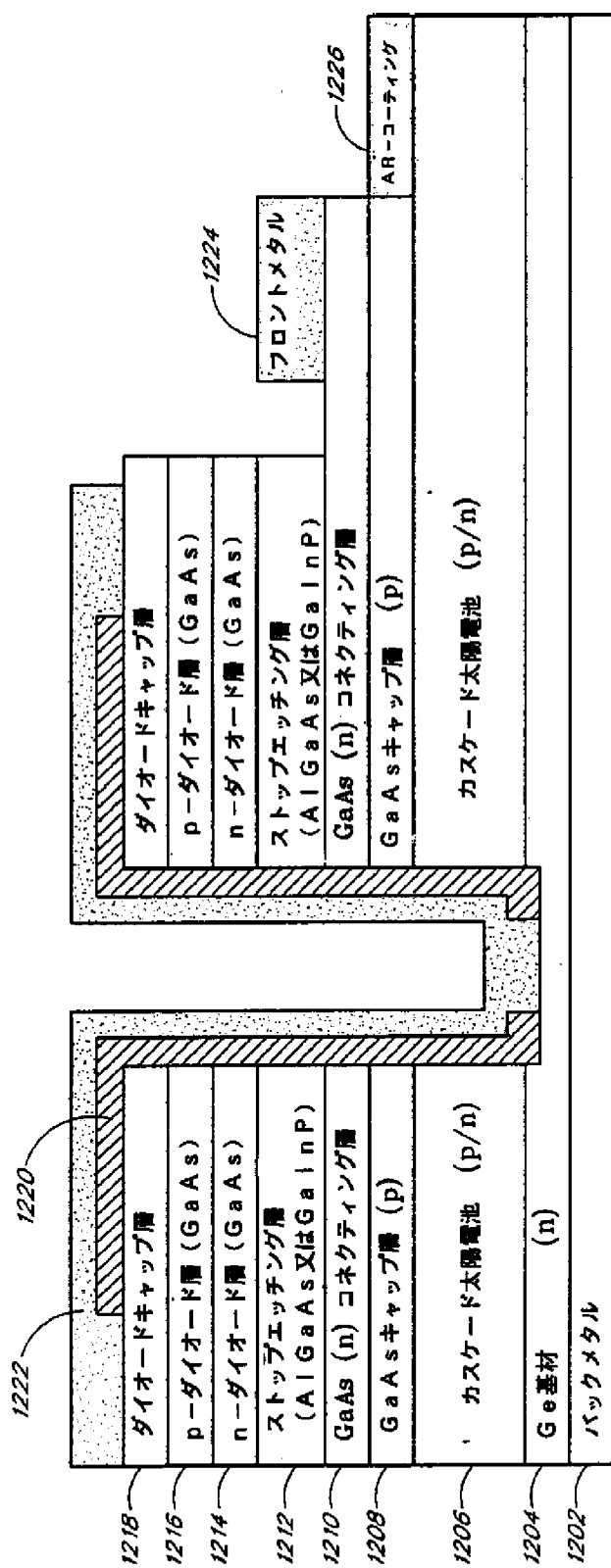


FIG. 11

[Drawing 12]



[Drawing 13]

FIG. 12

FIG. 13A

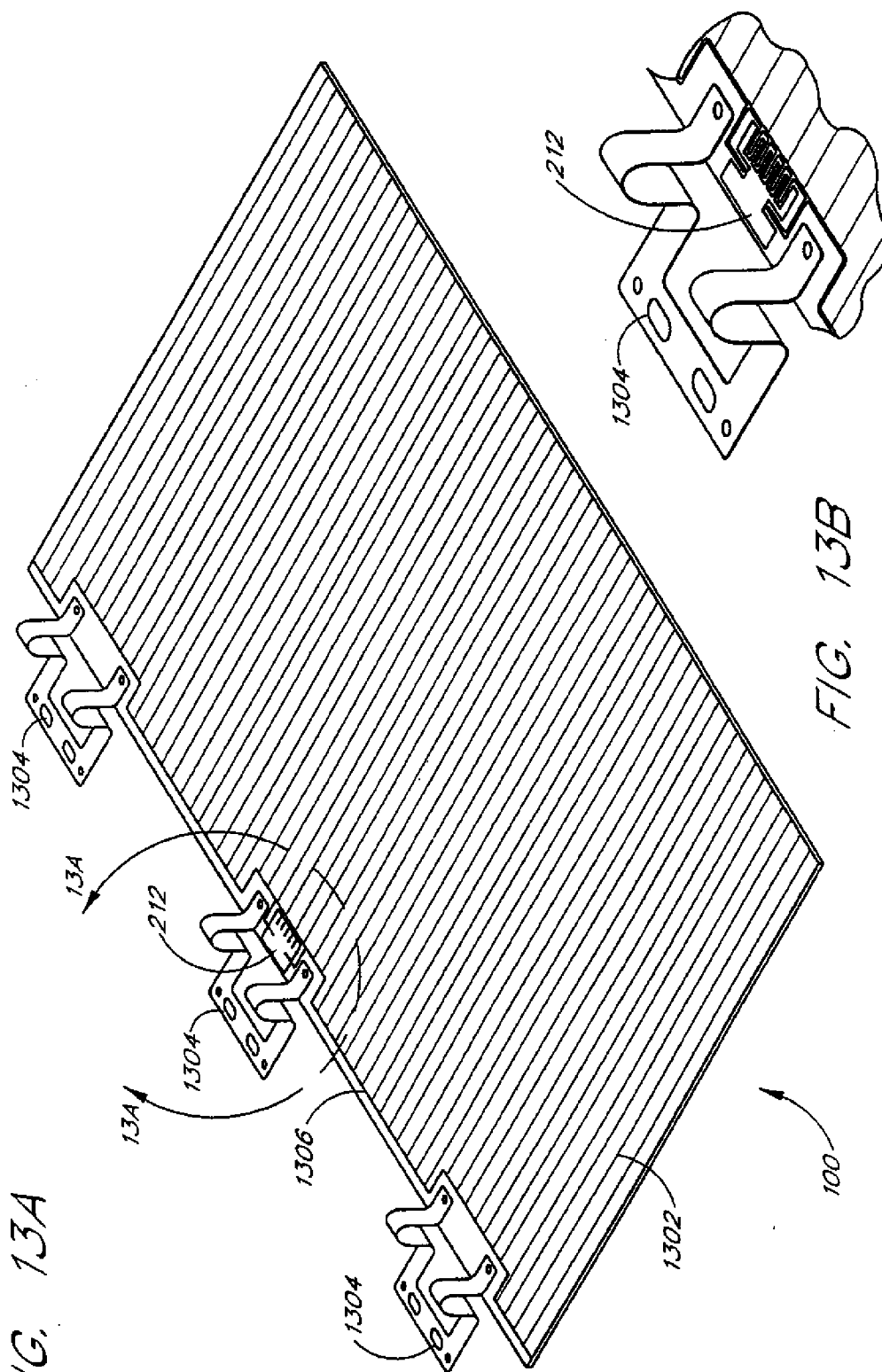
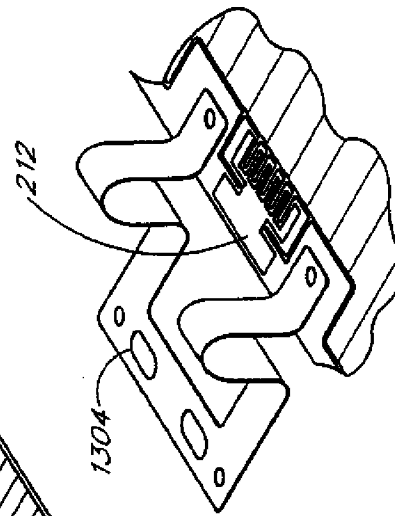


FIG. 13B



[Drawing 14]

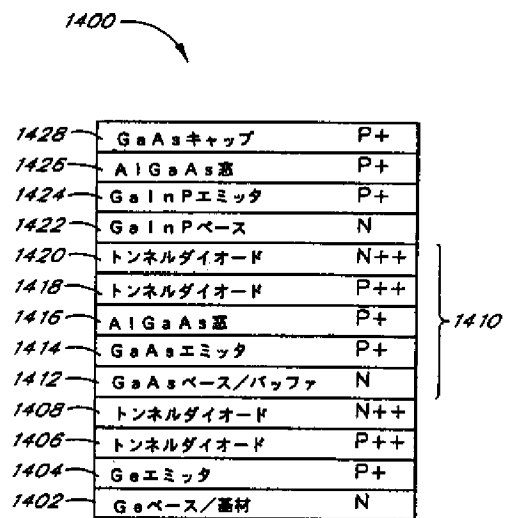


FIG. 14A

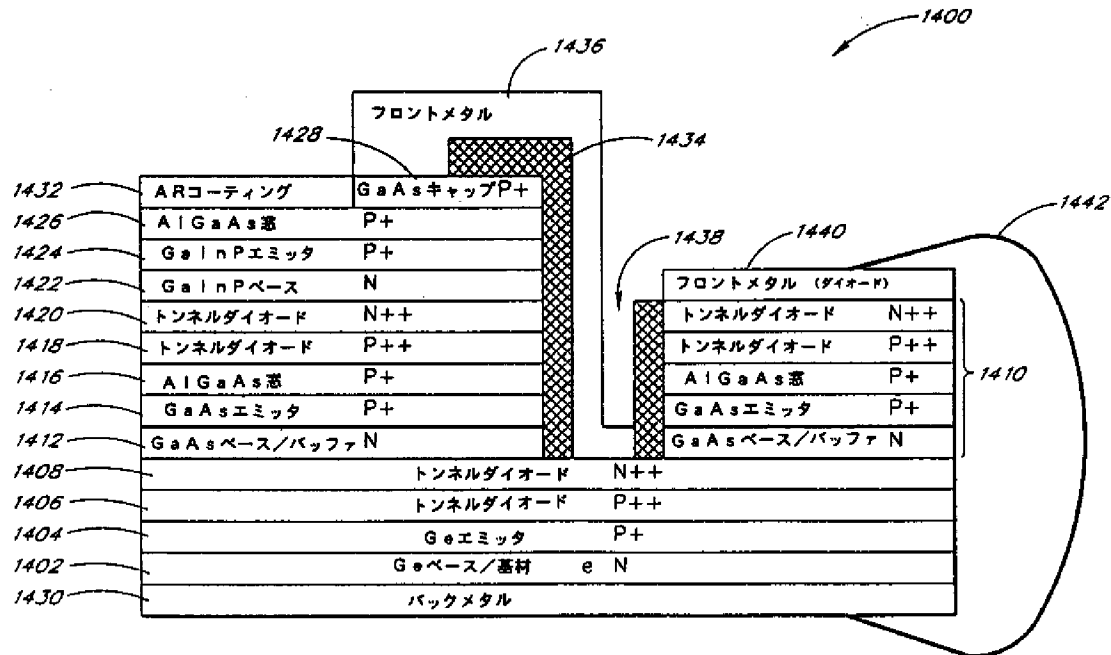


FIG. 14B

[Drawing 15]



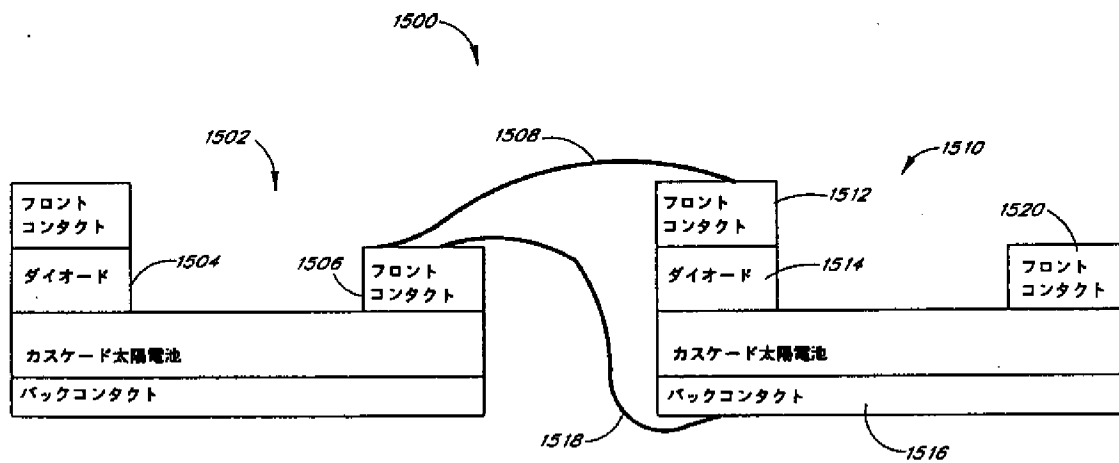


FIG. 15A

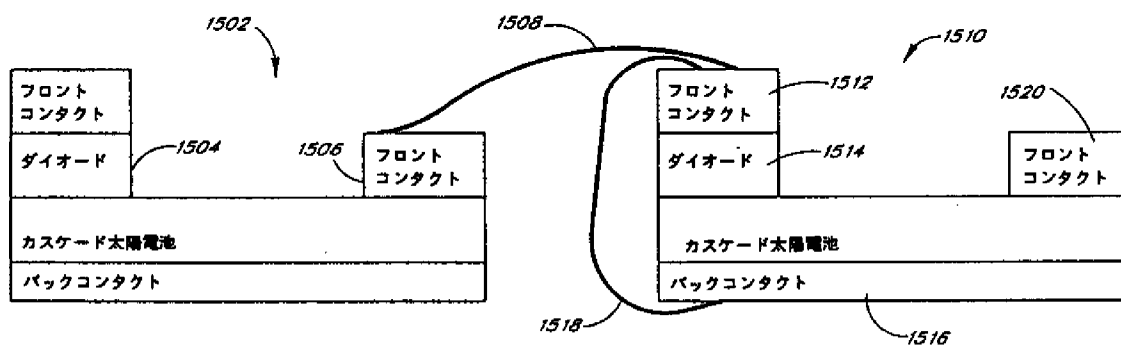


FIG. 15B